REMARKS

The Examiner's Action mailed on August 10, 2005 and Advisory Action mailed on December 15, 2005 have been received and their contents carefully considered. Additionally attached to this Amendment is a Request for Continued Examination, together with the applicable fee.

In this Amendment, Applicants have added claims 18-19 to further protect the disclosed invention. Claims 1, 17, and 18 are independent claims. Claims 1-19 are now pending in the application. All of the amendments can find support from the disclosures of the present application; thus, no new matter introduced by the amendments. The amendment to claim 4 is the same as those in the November Amendment After Final Rejection, which the Applicants assume was not entered (box 7 in the Advisory Action was not checked), and should overcome the §112 rejection.

For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-11, 14, and 17 are rejected under 35 U.S.C. 102 (e) as being anticipated by *Jain* (US Patent 6,275,088). It is submitted that claim 1 clearly is patentable over *Jain* for at least the following reasons. The Applicant's independent claim 1 recites:

> Claim 1 (Currently amended): An apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:
>
> a comparator, coupled to the transmission line, for comparing a line signal of the transmission line with an **inputted** reference voltage, and accordingly outputting a comparison signal;

a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;

a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;

a constriction controller, coupled to the comparator, for outputting a constriction signal; and

a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source;

wherein when the level of the line signal changes from a first voltage level to a second voltage level, the level of the constriction signal successively is changed from a third voltage level to a fourth voltage level, maintains the fourth voltage level for a period, and returns to the third voltage level.

Jain recites:

> Turning now to FIG. 5, a schematic diagram of one embodiment of the clamping circuit 22 is illustrated. The transmission line 16 is connected to an input buffer 36, which is comprised of two inverters 50, 51. [emphasis added; see *Jain*'s col. 4, lines 7 to 10, and Fig. 5]

The Examiner views *Jain*'s input buffer 36, which is comprised of two inverters 50, 51, as the comparator defined in claim 1. With respect, a person skilled in the art will consider a buffer quite a different electrical component from a comparator, and a comparator can not be anticipated by a buffer. The intrinsic thresholds of the inverters can not be adjusted by the user, while the input signals to the two input end of the comparator can be chosen by the user. That is, the inputted reference voltage can be well selected by the user to minimize the probability of reading error. For example, if

the inputted reference voltage is chosen to be higher than the general ring-back points B as shown in Fig. 3B, or, chosen to be larger than Vtt/2, the probability of reading error can be further reduced. Based on the fact that the inputted reference voltage of the comparator can be chosen by the user while the intrinsic thresholds of the inverters is fixed after the inverters are manufactured, the comparator defined in claim 1 cannot be anticipated by *Jain*'s input buffer 36, which is comprised of two inverters 50, 51. Claim 1 therefore is respectfully submitted to be patentable over *Jain*.

Claims 2-16 depend from claim 1, and therefore are patentable for at least the reasons advanced above as to the patentability of claim 1. Claim 17 is also patentable based on the same reasons recited for claim 1 above.

In addition, it is submitted that new claim 18 is patentable over *Jain* for at least the following reasons. Applicant's independent claim 18 recites:

> Claim 18 (New): An apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect, the apparatus comprising:
>
> a comparator, coupled to the transmission line, for comparing a line signal on the transmission line with a reference voltage, and accordingly outputting a comparison signal;
>
> a termination controller, coupled to the comparator, for outputting a termination control signal according to the comparison signal;
>
> a termination variable resistor, coupled to a termination voltage and the transmission line, the resistance of the termination variable resistor being adjusted according to the termination control signal for providing a voltage to the transmission line;
>
> a constriction controller, coupled to the comparator, for outputting a constriction signal; and
>
> a transistor, having a gate and a source, the gate receiving the constriction signal, the transistor being coupled to a constriction voltage and the transmission line, the resistance of the transistor being adjusted according to the voltage difference between the gate and the source;

wherein when the level of the line signal changes from a high voltage level to a low voltage level, the level of the constriction signal successively is changed from a first voltage level to a second voltage level to turn on the transistor, maintains the second voltage level for a period, and returns to the first voltage level;

wherein after the level of the line signal changes from the **high** voltage level to the **low** voltage level, **the transistor is turned on to provide the constriction voltage to the transmission line**, so that the level of the transmission line is pulled up to reduce the undershot and thus the ring-back effect is constricted;

wherein the constriction voltage is **larger** than the low voltage level.

Jain recites:

> Subsequently, the waveform on the transmission line 16 transitions to a low state, forcing the node A to a low state, while the output of the delay circuit 40 remains in its low state. Thus, the PMOS transistor 80 remains biased "on" by the output of the delay circuit 40, and the PMOS transistor 84 is likewise biased "on" by the low state at the node A. With the transistors 80, 84 biased "on," the voltage supply V_{supply} is connected to the gate of the NMOS transistor 34, biasing the transistor 34 "on." With the transistor 34 biased "on," the transmission line 16 is pulled toward **ground** to counteract the ringing present on the transmission line 16.
>
> After the delay induced by the delay circuit 40, the output of the delay circuit 40 transitions to a high state, biasing the PMOS transistor 80 "off" and the NMOS transistor 82 "on." With the transistor 82 biased "on," the gate of the NMOS transistor 34 is again pulled to ground and biased "off." Thus, a high-to-low transition in the waveform on the transmission line 16 induces the NMOS transistor 34 to be biased "on" for a period of time corresponding to the delay of the delay circuit 40.

In Jain's clamping circuit 22, transistor 34 is coupled between the transmission line 16 and the **ground** (see Fig. 5). When a high-to-low transition on the transmission line 16 occur, the transistor 34 is biased "on," and the transmission line 16 is pulled

toward **ground** to counteract the ringing present on the transmission line 16. That is, when a high-to-low transition on the transmission line 16 occurs, the transistor 34 is on, and the transmission line 16 is forced to couple to **ground**, which is substantially **equal** to the voltage level of the low state of transmission line 16. Jain does not disclose "the transistor being coupled to a constriction voltage and the transmission line", "after the level of the line signal changes from the high voltage level to the low voltage level, the transistor is turned on to provide the constriction voltage to the transmission line, so that the level of the transmission line is pulled up to reduce the undershot and thus the ring-back effect is constricted", and "the constriction voltage is **larger** than the low voltage level". Therefore, claim 18 is not anticipated by *Jain*. With respect, claim 18 is patentable over *Jain*.

Furthermore, it is submitted that the added claim 19 is patentable over *Jain* for at least the following reasons. Applicant's independent claim 19 recites:

> Claim 19 (New): The apparatus according to claim 18, wherein the constriction voltage is larger than the termination voltage.

Jain's transistor 34 is coupled between the transmission line 16 and the ground, therefore Jain discloses neither "the transistor being coupled to a constriction voltage and the transmission line" as recited in claim 18, nor "the constriction voltage is larger than the termination voltage" as recited in claim 19. Therefore, claim 19 is not anticipated by *Jain* and, with respect, is patentable over *Jain*.

Based on the above, the rejections under §§ 112, 102, and 103 having been addressed, it is submitted that the application is in condition for allowance, and such a Notice, with allowed claims 1-19, earnestly is solicited.

If the Examiner believes that a further conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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Date

Nick Bromer

Nick Bromer (Reg. No. 33,478)
(717) 426-1664
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924